Selection Criteria:

Selection of participants will be done on '**First Come First Serve Basis'**. Organizing committee's decision will be final in selecting the participants.

Important Dates:

Last Date for Registration/DD: 31st May 2019

Notification of Selection: 3rd June 2019

Important Links:

For Registration: http://sttp.spit.ac.in/
Email: sttp@spit.ac.in

Other: *www.spit.ac.in*

Venue:

Sardar Patel Institute of Technology
Bhavan's Campus, Munshi Nagar,
Andheri (W), Mumbai 400 058
Tel: 91-22-2670 8520, 26707440, 2628 7250
Fax No.: 91-22-26701422

How to Reach:

1. By Air: Santacruz Airport (5 Km)
2. By Train: Andheri Station (1.5 Km)
3. By Metro: Azadnagar Station (0.5 Km)
4. By Bus From Andheri (W) station: 249/250/254/257/259

Patrons:

Prof. S. G. Chitale, Director
Dr. Prachi Gharpure, Principal

Dr. Y.S. Rao, Dean R & D

Coordinator:

Dr. Surendra Rathod

Phone: 26707440/26708520 Extn. 350

Mobile: 9920228275

Email: surendra_rathod@spit.ac.in

Organizing Committee:

1. Dr. Rajendra Sutar
2. Dr. Deepak Karia
3. Prof. K. T. Talele
4. Prof. Narendra Bhagat
5. Prof. Prashant Kasambe
6. Prof. Govind Haldankar
7. Prof. Manisha Bansode
8. Prof. Payal Shah
9. Prof. Priya Deshpande
10. Prof. Najib Ghatte
11. Prof. Jayashree Rathod
12. Prof. Kumar Khandagale
13. Prof. Nikunj Parikh
14. Prof. Minal Khobragade

Bharatiya Vidya Bhavan's
Sardar Patel Institute of Technology

Announces

AICTE Sponsored One Week STTP on

"Front End VLSI Design and Verification"

24th June 2019 to 29th June 2019

Organized by

Department of Electronics Engineering,
Sardar Patel Institute of Technology,
Munshi Nagar, Andheri (W),
Mumbai 400 058
Tel: 91-22-2670 8520, 26707440, 2628 7250
Fax No.: 91-22-26701422
www.spit.ac.in
Email: sttp@spit.ac.in

About us

Sardar Patel Institute of Technology is autonomous institute affiliated to the University of Mumbai. Institute runs four UG, three PG and four Ph.D. programmes. NIRF ranked S.P.I.T. at 114. Department of Electronics Engineering has earned a great reputation in the field of engineering education, as well as industry. The department has well equipped laboratories to cater the curriculum. The department regularly organizes value added courses and STTPs. Department is provisionally accredited by National Board of Accreditation. Department faculty are always eager to learn new technologies and implement innovative methodologies for teaching learning for better student engagement.

About the STTP

The Front end VLSI design has achieved tremendous growth in worldwide markets since last few decades. There is a significant gap between the actual requirements of industry and the knowledge imparted in academics about the Physical System Implementation on FPGA and their verification strategies. It is very important and necessary to share the experiences of FPGA Design flow and Verification from the experts. There is a need for upgradation of the curriculum to enhance skills in Physical Design Implementation and Verification.

Through this Short term training program we aim to bring the industry expertise to the doors of academia to develop Physical Design, Implementation and Hardware Verification skills necessary to effectively accomplish design of VLSI Systems. Candidates will gain hands-on experience on Xilinx family FPGA's.

Course Contents/Highlights:

Broadly one week STTP will cover following contents:

- Verilog Hardware Description language
- Synthesis and Physical Implementation
- Implementation on Zybo and Nexys-4 DDR
- Using Microblaze Soft Core
- Fundamentals of Verification
- SystemVerilog Fundamentals
- Object Oriented Programming in Verification
- Advanced verification concepts like Randomization, Inter Process Communication, Code Coverage and Assertion
- Testbench writing using SystemVerilog
- Various Toolsets for Verification

Objectives of the STTP

1. Identification of challenges in VLSI System design, Functional testing and Hardware verification.
2. Development of trained resources in VLSI System design and verification.
3. To acquire insights about technological details of VLSI system Design flow from industry experts
4. To motivate teachers to develop curriculum and pedagogy for VLSI System Design and Verification.
5. To discuss the methodologies of selection of particular families of FPGA for specific application to reduce design complexity.

Teachers from AICTE recognized engineering colleges and polytechnics can attend this seminar.

Resource Persons:

Distinguished faculty members from the renowned institutes like IIT, industries and other institutes will be the resource persons for the Seminar.

Registration:

This being AICTE sponsored STTP there are **NO registration charges**. However nominal amount of Rs. 2500/-- in the form of Cash or Demand Draft in favor of "Principal, Sardar Patel Institute of Technology" payable at Mumbai is taken as deposit. Cash or Demand draft should reach to us on or before 31st May 2019 along with online registration. For online registration please visit **http://sttp.spit.ac.in/**.

Demand Draft/Cash taken as deposit will be returned if not selected or on successful completion of STTP. DD/Cash will not be returned if candidate is selected and does not attend the STTP.

Contact for Registration:

Prof. Payal Shah
Dept. of Electronics Engg.,
Phone: 26707440/26708520 Ext. 356
Mobile: 9867368965
Email: payal_shah@spit.ac.in

About Accommodation and TA:

Please note that only outside Mumbai participants (staying beyond Mumbai, Navi Mumbai and Thane), will be paid maximum upto Rs. 500 per day. Travel by 3-tier AC will be reimbursed to outstation participants as per the norms.

Contact for Accommodation:

Prof. Narendra Bhagat Mobile: 9892365664
Email: narendra_bhagat@spit.ac.in