Bharatiya Vidya Bhavan's

SARDAR PATEL INSTITUTE OF TECHNOLOGY

MUNSHI NAGAR, ANDHERI (WEST), MUMBAI - 400 058

(Autonomous Institute Affiliated to University of Mumbai)

Schedule for AICTE Sponsored One Week STTP on "Front End VLSI Design and Verification" (24th June 2019 to 29th June 2019)

Registration on 24th June: 8.00 am to 9.00 am

Inauguration on 24th June: 9.00 am to 9.30 am

Venue: Room No: 008 (Ground Floor) and 305 (3rd Floor)

Date	9.30 am to 11.00 am	11.15 am to 12.45 pm	1.45 pm to 3.15 pm	3.30 pm to 5.00 pm
(Tea Break: 11.00 am to 11.15 am, Lunch: 12.45 pm to 1.45 pm)				
24th June 2019	Introduction to VLSI Testing and Verification (Dr. Virendra Singh, IITB)	Xilinx ISE and Vivado System Design Flow (Prof. Kumar Khandagale, S.P.I.T.)	Verilog HDL, Synthesis and Physical Implementation (Prof. Kumar Khandagale, S.P.I.T.)	
25th June 2019	Evaluation of verification in digital IC flow (Mr. Damodara Sambashiva, Entuple Technologies, Bengaluru)	HDL based verification pros and cons and flow (Mr. Damodara Sambashiva, Entuple Technologies, Bengaluru)	Basic HDL verification flow using incisive (Mr. Damodara Sambashiva, Entuple Technologies, Bengaluru)	Coverage analysis in verification (Mr. Damodara Sambashiva, Entuple Technologies, Bengaluru)
26th June 2019	Need for HVL based verification and advantages of SystemVerilog over Verilog HDL (Mr. Harish K. S. , Entuple Technologies, Bengaluru)	HVL based verification flow using incisive (Mr. Harish K. S. , Entuple Technologies, Bengaluru)	Functional coverage and randomization using SV (Mr. Sumit Patil , Entuple Technologies, Pune)	
27th June 2019	Overview of verification methodologies (Mr. Harish K. S. , Entuple Technologies, Bengaluru)	Introduction to UVM (Mr. Harish K. S. , Entuple Technologies, Bengaluru)	Demo on UVM based verification (Mr. Sumit Patil, Entuple Technologies, Pune)	
28th June 2019	SystemVerilog Concepts: OOP approach, IPC, Randomization, Code Coverage and Assertions (Dr. S.S. Rathod, S.P.I.T.)	Microblaze Soft Core and High Level Synthesis (Prof. Mrugendra Vasmatkar, VESIT)	Implementation of Microblaze Soft Core processor on Zybo and Nexys-4 DDR Platform (Prof. Mrugendra Vasmatkar, VESIT)	
29th June 2019	HDL Coder Workflow for Digital Down Convertor (Mr. Pawan Fakatkar, Mathworks, Bengaluru)	Hardware in Loop Implementation and Verification (Mr. Pawan Fakatkar, Mathworks, Bengaluru)	Skill attainment Test, Quiz and Feedback (Program Evaluation Committee)	**Valedictory**