Bharatiya Vidya Bhavan's
SARDAR PATEL INSTITUTE OF TECHNOLOGY
MUNSHI NAGAR, ANDHERI (WEST), MUMBAI - 400 058
(Autonomous Institute Affliated to University of Mumbai)

AICTE Sponsored Three Two Week FDP on "VLSI Design Using Cadence Tools"

Tentative Schedule

STTP1: Digital CMOS Design and Verification
STTP2: Analog CMOS VLSI Design
STTP3: Mixed Signal VLSI Design

Timings:

Inauguration: 9.30 to 10.00 am
Morning Sessions: 10.00 am to 1.00pm
Evening Sessions: 5.00pm to 7.00pm

Please note based on resource persons availability there may be changes in timings on few days.

STTP1: Digital CMOS Design and Verification
(12th Oct to 17th Oct)

Date	Contents		
12th Oct	**Keynote**-Introduction to VLSI and Industry Overview (Mr. Sarang Shelke, Engineering Director at Tensilica IP Group Cadence Design Systems)	Basic CMOS Digital Design and Calculating Logical Effort of Gates (Dr. Naushad Alam, AMU)	Circuit simulation and analysis methods (Dr. Naushad Alam, AMU)
13th Oct	Digital Design Stages, Modeling using Verilog, Modeling of Sequential Logic Circuits - Guidelines (Entuple)	Design of Combinational Logic circuits using Verilog, Sequential Logic Circuits Modeling and Simulation – DEMO (Entuple)	Simulation & Analysis of Combinational Logic Circuits using Incisive Simulator (Entuple)
14th Oct	Design of State Machines, Memories & Functional Verification (Entuple)	Protocol Verification :AMBA APB Protocol - Project Case Study Discussion (Entuple)	APB based memory design & verification (Entuple)
15th Oct	Challenge in CMOS Digital Design (Dr. Sudeb Dasgupta, Professior IIT Roorkee)	Research Opportunities in VLSI (Dr. Sudeb Dasgupta, Professior IIT Roorkee)	Verilog HDL, Synthesis and Physical Implementation (Mr. Kumar Khandagale, Edelweiss Securities Ltd.)
16th Oct	High Speed Digital Design with Low Power Approach (Dr. Shaila Subbaraman)	High Speed Digital Design with Low Power Approach (Dr. Shaila Subbaraman)	Layout capture and LVS verification (Dr. Naushad Alam, AMU)
17th Oct	Skill attainment Test, Feedback and Valedictory Session		

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STTP2: Analog CMOS VLSI Design
(2nd Nov to 7th Nov)

Date	Contents
2nd Nov	Fundamentals of Analog CMOS Small signal modeling
3rd Nov	Analog/Custom IC Design and Analysis Cadence Virtuoso Analog Design Environment (Entuple)
4th Nov	Standard Cell Design and Characterization using Cadence Virtuoso and Spectre (Entuple)
5th Nov	Single Stage Amplifier Circuit Topologies, Diff-Amp, Op-Amp Design
6th Nov	Noise, Frequency response and layout. Circuit Simulation. Post-layout simulation and LVS
7th Nov	Skill attainment Test, Feedback and Valedictory Session

STTP3: Mixed Signal VLSI Design
(30th Nov to 5th Dec)

Date	Contents
30th Nov	Fundamentals of Mixed Signal Design Switch capacitor circuits
1st Dec	Analog a& Mixed Signal Design (Entuple)
2nd Dec	AMS Design and Simulation Using Cadence Virtuso & Spectre (Entuple)
3rd Dec	Oscillators and PLL
4th Dec	ADC and DAC, Case studies
5th Dec	Skill attainment Test, Feedback and Valedictory Session