ABOUT THE INSTITUTE AND DEPARTMENT

Bharatiya Vidya Bhavan's Sardar Patel Institute of Technology is an autonomous institute affiliated to the University of Mumbai. Institute runs four UG, three PG and four Ph.D. programmes in engineering. NIRF ranked S.P.I.T. consistently between 100 to 150. Institute has strong culture of innovation, research and entrepreneurship. S.P.I.T. is consistently achieving 100% placements since few years.

Department of Electronics Engineering has earned a great reputation in the field of engineering education, as well as industry. Department has well equipped laboratories to cater the unique, flexible and globally competent curriculum. Department regularly organizes value added courses and STTPs. Department is provisionally accredited by National Board of Accreditation consistently in last three accreditation cycles.. Department has highly motivated faculty members. Department has Ph.D. research centre in Electronics Engineering. Strong research and innovation culture makes the department one of the highly sought after department for pursuing B.Tech and Ph.D. Students of the department every year shine in national level competitions like Texas Instruments, E-Yantra, Robocon and Hackathons. Department alumni are presently working in many core companies like INTEL, Apple, Samsung, Microsoft etc.

REGISTRATION PROCESS

This being AICTE sponsored STTP there are **NO registration charges**. However online registration is compulsory. Please visit **http://sttp.spit.ac.in/**. **You can register for one or more than one FDP. For certificate attendance and passing of Examination is mandatory.**

CONTACT FOR REGISTRATION

Prof. Payal Shah (Mobile: 9867368965)

Prof. Manisha Bansode (Mobile: 9820962072

IMPORTANT DATES & LINKS

Last date for registration:

STTP1: 30th Sep2020

STTP2: 18th Oct 2020

STTP3: 7th Nov 2020

For Registration: http://sttp.spit.ac.in/

Email: sttp@spit.ac.in

Other: *www.spit.ac.in*

STTP SCHEDULE

STTP1	STTP2	STTP3
Digital VLSI Design and Verification	Analog CMOS VLSI Design	Mixed Signal VLSI Design
12th Oct to 17th Oct	2nd Nov to 7th Nov	30th Nov to 5th Dec

WHO SHOULD ATTEND THE COURSE

Teachers from AICTE approved academic and research institutions can attend this course. This course if particularly useful for teachers working/teaching or doing research in the domain of VLSI Design

AICTE Sponsored Three ONE week Online Short Term Training Programme (STTP) On

"VLSI Design Using Cadence Tools"

12th Oct- 5th Dec 2020

Coordinator

Dr. Surendra Rathod

Professor

Electronics Engineering Department

Organized By

Electronics Engineering Department

Bharatiya Vidya Bhavan's

Sardar Patel Institute of Technology,

(An autonomous institution affiliated to University of Mumbai)

Mumbai, Maharashtra

Telephone: 91-22-26707440 / 26287250 |

URL : www.spit.ac.in

ABOUT STTP

VLSI design has achieved tremendous growth in worldwide markets since last few decades. There is a significant gap between the actual requirements of industry and the knowledge imparted in academics on the industry grade toolsets. The main objective of this training is to provide information through demonstrations of digital and analog blocks. Theoretical background will be supported by demonstrations on various simulation tools including Cadence toolsets. The aspects of Digital VLSI Design, Analog VLSI Design, Mixed Signal Design, various analysis, layout, DRC, Layout versus Schematic, parasitic extraction, post layout simulation to be demonstrated in the course. Through this STTP we aim to give information which is necessary to effectively accomplish design of VLSI Systems. This STTP also aims to share the experiences of professionals working in the domain of VLSI Design.

STTP OBJECTIVES

1. Identification of challenges in VLSI design and simulation of digital and analog circuits.
2. Development of trained resources in VLSI design.
3. To acquire insights about technological details of VLSI system Design flow from industry experts
4. To motivate teachers to develop and curriculum and pedagogy for VLSI Design.
5. To provide information about tools used in VLSI Industry

RESOURCE PERSONS

Distinguished faculty members from the renowned institutes like IIT, other institutes and industry will be the resource persons for the STTP.

CADENCE TOOL ACCESS

Optional access to Cadence tools for hands-on session may be provided by Entuple to interested participants on payment basis. For this please contact Entuple Representatives.

STTP MAJPOR CONTENTS

Broadly Three one week STTPs will cover the following contents:

- Introduction to VLSI and Industry Overview
- VLSI Design Flow
- Invited talks delivered by experts from industry and academic organizations
- Demonstrations through simulations.

STTP1: Digital VLSI Design and Verification

ASIC design flow, Modeling using Verilog, Function simulation to Synthesis. Simulation and analysis using Cadence incisive simulator. Circuit simulation, layout capture and LVS verification, Physical Design and Verification Overview. Basics of CMOS digital design, Case studies and research challenges.

STTP2: Analog CMOS VLSI Design

Characterization of Analog Model Parameters, Single Stage Amplifier Circuit Topologies, Diff-Amp and Op-Amp Design, Exposure to Cadence Virtuoso Analog Design Environment

STTP3: Mixed Signal VLSI Design

Fundamentals of Mixed Signal Design with Examples, Case studies, Exposure to simulation toolset for mixed signal design

Expected Outcome

1. Manpower development in the area of design of Front End and back end VLSI Design
2. Interaction among peers in the field of Physical Design and Verification.
3. Course material related to VLSI Design on concepts taught during course
4. Development of laboratory exercises related to digital, analog and mixed signal CMOS VLSI design
5. Sharing of knowledge among participants about advanced VLSI design concepts
6. Exposure to industry standard toolsets for digital, analog and mixed Signal design

PATRON

Dr. Shesha Iyer — Chairman, BoG, S.P.I.T

Dr. B. N. Chaudhari — Principal, Sardar Patel Institute of Technology

ORGANIZING COMMITTEE

Dr. Surendra Rathod (Coordinator)

Prof. Narendra Bhagat

Prof. Prashant Kasambe

Prof. Manisha Bansode

Prof. Payal Shah

Prof. Priya Deshpande

Prof. Sneha Weakey

Shri. Shrikant Goswami

PROGRAMME EVALUATION COMMITTEE

1. Dr. B. N. Chaudhari
   Principal of the Institution (Chairperson)
2. Dr. Deepak Karia
   Head of Electronics Engineering Department
3. Dr. Reena Sonkusare
   Head of Electronics & Telecom Engg. Department
4. Dr. Sukanya Kulkarni
   Subject Expert
5. Dr. S. S. Rathod
   Co-ordinator of the program (Member Secretary)