Bharatiya Vidya Bhavan's
SARDAR PATEL INSTITUTE OF TECHNOLOGY
MUNSHI NAGAR, ANDHERI (WEST), MUMBAI - 400 058
(Autonomous Institute Affliated to University of Mumbai)

AICTE Sponsored Three ONE Week STTP on "VLSI Design Using Cadence Tools"

Schedule

STTP1: Digital CMOS Design and Verification
STTP2: Analog CMOS VLSI Design
STTP3: Mixed Signal VLSI Design

Timings:

Inauguration: 9.30 to 10.00 am
Morning Sessions: 10.00 am to 1.00pm
Evening Sessions: 5.00pm to 7.00pm
Please note Evening sessions by Entuple are from 2 or 4 pm.

STTP1: Digital CMOS Design and Verification (12th Oct to 17th Oct)

Date	Contents		
12th Oct	**Keynote**- The Evolution and Future Trends In Semiconductors & Electronics (Mr. Sarang Shelke, Engineering Director at Tensilica IP Group Cadence Design Systems)	High Speed CMOS Logic Design (Dr. Naushad Alam, AMU)	Circuit simulation and analysis methods (Dr. Naushad Alam, AMU)
13th Oct	Digital Design Stages, Modeling using Verilog, Modeling of Sequential Logic Circuits - Guidelines (Entuple)	Design of Combinational Logic circuits using Verilog, Sequential Logic Circuits Modeling and Simulation – DEMO (Entuple)	Simulation & Analysis of Combinational Logic Circuits using Incisive Simulator (Entuple) **Time: 2 to 4 pm**
14th Oct	Design of State Machines, Memories & Functional Verification (Entuple)	Protocol Verification :AMBA APB Protocol - Project Case Study Discussion (Entuple)	APB based memory design & verification (Entuple) **Time: 2 to 4 pm**
15th Oct	Challenge in CMOS Digital Design (Dr. Sudeb Dasgupta, Professior IIT Roorkee)	Research Opportunities in VLSI (Dr. Sudeb Dasgupta, Professior IIT Roorkee)	Verilog HDL, Synthesis and Physical Implementation (Mr. Kumar Khandagale, Edelweiss Securities Ltd.)
16th Oct	High Speed Digital Design with Low Power Approach (Dr. Shaila Subbaraman, WCE)	High Speed Digital Design with Low Power Approach (Dr. Shaila Subbaraman, WCE)	Layout capture and LVS verification (Dr. Naushad Alam, AMU)
17th Oct	Skill attainment Test, Feedback and Valedictory Session		

Bharatiya Vidya Bhavan's
SARDAR PATEL INSTITUTE OF TECHNOLOGY
MUNSHI NAGAR, ANDHERI (WEST), MUMBAI - 400 058
(Autonomous Institute Affliated to University of Mumbai)

STTP2: Analog CMOS VLSI Design
(2nd Nov to 7th Nov)

Date	Contents		
2nd Nov	**Keynote:** Analog CMOS Design (Dr. Mohd. Hasan AMU)	Fundamentals of Analog CMOS Design (Dr. Mohd. Hasan AMU)	Analog Circuit Simulation (Dr. Naushad Alam AMU)
3rd Nov	Analog Circuit Design Principles (Entuple)	Design of an Operational Amplifier for the given specifications (Entuple)	Schematic Capture, Simulation & Analysis using Cadence Virtuoso & Spectre (Entuple) **Time: 2 to 4 pm**
4th Nov	Analog Layout Design Principles and guidelines (Entuple)	Analog Layout Design Principles and guidelines (Entuple)	Analog Layout Design for the given specifications (Entuple) **Time: 2 to 4 pm**
5th Nov	Amplifier Circuit Topologies (Dr. S. S. Mande, DBIT)	Nanoscale op-amp design(Dr. S. S. Mande, DBIT)	Implementation of Communication Circuits Using Current Mode Technique (Prof. Narendra Bhagat S.P.I.T.)
6th Nov	Analog Circuit Design for Sensor Interface (Dr. Pramod Murali, IITB)	Analog Circuit Design for Sensor Interface (Dr. Pramod Murali, IITB)	Post-layout simulation and LVS (Dr. Naushad Alam, AMU)
7th Nov	Skill attainment Test, Feedback and Valedictory Session		

Bharatiya Vidya Bhavan's
SARDAR PATEL INSTITUTE OF TECHNOLOGY
MUNSHI NAGAR, ANDHERI (WEST), MUMBAI - 400 058
(Autonomous Institute Affliated to University of Mumbai)

STTP3: Mixed Signal VLSI Design
(30th Nov to 5th Dec)

Date	Contents		
30th Nov	**Keynote:-**Mixed Signal Circuits and Systems: Emerging Applications (Dr. Maryam Shojaei Baghini, IITB)	Switch Capacitor Circuits (Dr. Maryam Shojaei Baghini, IITB)	Implementation of DSP Algorithms in VLSI (Dr. Shaila Subbaraman, WCE.)
1st Dec	Synthesis and Pre-Layout STA (Entuple)	Physical Design & Verification flow - Industry perspective (Entuple)	Demo : Logic Synthesis and Pre- Layout STA using Cadence Genus Demo: Getting started with Physical Design using Cadence Innovus (Entuple) **Time: 2 to 4 pm**
2nd Dec	Concepts of Floor plan and Power plan & APR Clock Tree synthesis Physical Verification (Entuple)	Concepts of Floor plan and Power plan & APR Clock Tree synthesis Physical Verification (Entuple)	Demo :Placement & Routing of an SoC using Cadence Innovus Demo: Power, Timing Analysis signoffs using Cadence Voltus and Tempus (Entuple) **Time: 2 to 4 pm**
3rd Dec	Data Converters: ADC and DAC (Dr. S. Kumaravel, VIT Vellore)	Data Converters: ADC and DAC (Dr. S. Kumaravel, VIT Vellore)	Dynamic Offset Cancellation Techniques (Mr. Meraj Ahmed, Research Scholar, IITB)
4th Dec	Low Power Architectures for Signal Processing and Communications (Dr. Mohd. Hasan AMU)	Low Power Architectures for Signal Processing and Communications (Dr. Mohd. Hasan AMU)	Case Study on ADC and DAC (Dr. Shaila Subbaraman, WCE
5th Dec	Skill attainment Test, Feedback and Valedictory Session		