Bharatiya Vidya Bhavan's
Sardar Patel Institute of Technology,
(An autonomous institution affiliated to University of Mumbai)
Mumbai, Maharashtra

AICTE Sponsored STTP on VLSI Design Using Cadence Tools (Mode: ONLINE)

Welcome to participate in this exciting learning initiative of S.P.I.T. supported by AICTE New Delhi. You can register on https://sttp.spit.ac.in/ OR watch all sessions Live on the YouTube Channel.

Theme: Mixed Signal VLSI Design

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Date	Time	Details
30/11/2020	9.30 am to 10.00 am	Keynote: Memory Design: An Industry Perspective *(Dr. Abhishek A. Sharma, Components Research at Intel Corporation, Oregon, USA)*
30/11/2020	10.00 am to 11.30 am	Mixed Signal Circuits and Systems: Emerging Applications *(Dr. Maryam Shojaei Baghini, IITB)*
30/11/2020	11.45 am to 1.15 pm	Switch Capacitor Circuits *(Dr. Maryam Shojaei Baghini, IITB)*
30/11/2020	5.00 pm to 7.00 pm	Device, Circuit and Architectures for enhancing Hardware Security *(Dr. Ramesh Vaddi SRM University)*
01/12/2020	10.00 am t0 11.30 am	Full Custom and Semi-Custom IC Design Flow Overview - Tool perspective *(Entuple Technologies, Bengaluru)*
01/12/2020	11.45 am to 1.15 pm	Synthesis and Pre-Layout STA *(Entuple Technologies, Bengaluru)*
01/12/2020	2.00 pm to 4.00 pm	Physical Design & Verification flow - Industry perspective Demo : Logic Synthesis and Pre- Layout STA using Cadence Genus *(Entuple)*
02/12/2020	10.00 am 10 11.30 am	Floor plan and Power plan & APR, Clock Tree synthesis, Physical Verification Demo : Getting Started with Physical Design using Cadence Innovus *(Entuple)*
02/12/2020	11.45 am to 1.15 pm	Floor plan and Power plan & APR, Clock Tree synthesis, Physical Verification *(Entuple Technologies, Bengaluru)*
02/12/2020	2.00 pm to 4.00 pm	Demo :Placement & Routing of an SoC using Cadence Innovus Demo: Power, Timing Analysis signoffs using Cadence Voltus and Tempus *(Entuple)*
02/12/2020	5.00 pm to 7.00 pm	Secure Memory System Optimizations *(Dr. Prashant Nair, The University of British Columbia, Canada)*
03/12/2020	10.00 am to 11.30 am	Data Converters: ADC and DAC *(Dr. S. Kumaravel, VIT Vellore)*
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03/12/2020	5.00 pm to 7.00 pm	Dynamic Offset Cancellation Techniques *(Mr. Meraj Ahmed, Research Scholar, IITB)*
04/12/2020	10.00 am to 11.30 am	Low Power Architectures for Signal Processing and Communications *(Dr. Mohd. Hasan AMU)*
04/12/2020	11.45 am to 1.15 pm	Low Power Architectures for Signal Processing and Communications *(Dr. Mohd. Hasan AMU)*
04/12/2020	5.00 pm to 7.00 pm	Implementation of DSP Algorithms in VLSI *(Dr. Shaila Subbaraman, WCE)*
05/12/2020	2.00 pm to 3.00 pm	Mind Power *(Dr. Jagbir Singh, Mental Conditioning Trainer and Sports Psychologist)*